REMARKS

Applicants note there appears to have been no Examination of claim 14. Applicants have rewritten claim 14 in independent form including all the limitations of original claim 8 from which claim 14 depended and without adding any new limitations. Applicants request an examination of claim 14.

The Examiner rejected claims 1-20 under 35 U.S.C. 103 as being unpatentable over Steinmetz USP 5,600,579 in view of Lee USP 5,805,605.

Applicants respectfully traverse the §103 rejections with the following arguments.

35 USC § 103 Rejections

First, Applicants contend that there is no motivation for combining references. The Examiner states the motivation for combining references is "It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the semiconductor integrated device capable of selective execution as discussed in Lee, and to further provide a verification of the design utilizing a controlling test as discussed in Steinmetz in order to allow for reduced verification time." Applicants contend that this cannot a motivation for combining references.

Applicants contend that the combination of Steinmetz in view of Lee is incompatible because Steinmetz requires a design to simulate, but Lee supplies only hardware and hardware can not be used in conjunction with the software of Steinmetz.

Second, Applicants contend that claims 1, 8 and 15, as amended, are not obvious in view of Steinmetz in view of Lee because Steinmetz in view of Lee does not teach or suggest every feature of claims 1, 8 and 15.

In a first example, Steinmetz in view of Lee does not teach or suggest "wherein said I/O cores and said I/O controller are software descriptions of said integrated circuit design." The Examiner states that Lees discloses "the integrated circuit comprising an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit, design; (Lee. Column 4, Lines 1-11 Figure 4, Elements 2,4, 10, and 12)."

Applicants respectfully point out that Lee is disclosing a physical integrated circuit 32 comprised of a logic part 22, a switch part 24, a pad part 28 and a switch control part 30 and not an "integrated circuit design" Therefore, none of elements 2,4, 10, and 12 are "software descriptions of said integrated circuit design" as Applicants claims 1, 8 and 15 require.

In a second example, Steinmetz in view of Lee does not teach or suggest "A software system for verifying an integrated circuit design, said system comprising: an external memory mapped test device having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual I/O buses." The Examiner states that Lee discloses "an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models; (Lee. Column 4, Lines 12-22. Figure 4, Elements 1a-1d, 6, 8, and 16)."

Applicants respectfully point out that:

(1) Elements 1a, 1b and 1c (there is no 1d) are part of switch 24, elements 6 and 8 are part of memory 26 and element 16 is part of switch control 16, all of which are parts of the integrated circuit of Lee and none are parts of the "software system" are as Applicants claims 1, 8 and 15 require

(2) Applicants do not find in Lee "simulated I/O cores" or "I/O core models" as Applicants claims 1, 8 and 15 require, but rather physical cores.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 8 and 15 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance. Since claims 2-7 depend from claim 1, claims 9-14 depend from claim 8 and claims 16-20 depend from claim 15, Applicants respectfully maintain that claims 2-7, 9-15 and 16-20 are likewise in condition for allowance.

As to claims 2, 9 and 16, the Examiner states that "Lee, however, discloses the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external

memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules; each module containing a portion of said switch and connected to one of said I/O driver models. (Lee. Column 4, Lines 1-22. Figure 4)."

Applicants respectfully point out that Lee has no "external memory mapped test device modules" and no " I/O driver models." Applicants point out that switch control 30 is part of chip 32 and is hardware.

Based on the preceding arguments, Applicants respectfully maintain that claims 2, 9 and 16 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

As to claims 3, 10 and 17, the Examiner states that "Lee discloses the address register for setting said switch and controlling said I/O driver models. (Lee. Column 4, Lines 1-22. Figure 4)."

Applicants do not know what element of Lee the Examiner alleges is an address register and Applicants can find no address register in Lee column 4, lines 1-22 or FIG. 4). Further there no "I/O models" in Lee.

Based on the preceding arguments, Applicants respectfully maintain that claims 3, 10 and 17 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

As to claims 4, 11 and 18, the Examiner states that "Steinmetz discloses "wherein said integrated circuit design further includes an embedded processor for running said test operating said test operating system. (Steinmetz. Column 5, Lines 15-20, 37-46. Figure 1. Element 103, 115, 113, 107 and 101.)." Applicants point out that elements 103, 115, 113, 107 and 101 are part of Steinmetz's verification test system. Applicants point out that Steinmetz col. 5, lines 15-20,

37-46. is teaching that the verification system 100 comprises program modules (col. 5, lines 15-20) and the verification system can execute a test script having low level computer control col.37-46). There is no teaching the verification system includes an embedded processor. The computer that verification system 100 runs on includes a CPU, but that CPU is not part of the "integrated circuit design."

Based on the preceding arguments, Applicants respectfully maintain that claims 4, 11 and 18 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

As to claims 5, 11 and 18, the Examiner states that " Lee, however, discloses the address register for setting said portion of said switch and controlling said one I/O driver model. (Lee. Column 4, Lines 1-22. Figure 4)."

Applicants do not know what element of Lee the Examiner alleges is an address register and Applicants can find no address register in Lee column 4, lines 1-22 or FIG. 4.

Based on the preceding arguments, Applicants respectfully maintain that claims 5, 11 and 18 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

As to claims 6, 14 and 18, the Examiner states that "Steinmetz discloses an embedded processor for running said test operating system. (Steinmetz. Column 5, Lines 15-20, 37-46. Figure 1. Element 103, 115, 113, 107 and 101.)."

Applicants point out that elements 103, 115, 113, 107 and 101 are part of Steinmetz's verification test system. Applicants point out that Steinmetz col. 5, lines 15-20, 37-46. is teaching that the verification system 100 comprises program modules (col. 5, lines 15-20) and the verification system can execute a test script having low level computer control col.37-46).

There is no teaching the verification system includes an embedded processor. The computer that verification system 100 runs on includes a CPU, but that CPU is not part of the "integrated circuit design."

Based on the preceding arguments, Applicants respectfully maintain that claims 6, 11 and 18 are not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

As to claim 7, the Examiner states that "Lee, however, discloses the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design. (Lee, Column 4, Lines 1-22. Figure 4)."

Applicants maintain that Lee does not teach the elements the Examiner has listed based on Applicants arguments presented *supra* relative to claims 1-6, 8-13 and 15-20.

Based on the preceding arguments, Applicants respectfully maintain that claim 7 is not unpatentable over Steinmetz in view of Lee and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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Dated: 12/27/2005

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